Amendments to the Specification

Please delete the following paragraph under the title.

This application is a division of ~~Patent Application serial number~~ application No. 10/154,662, ~~filing date 5/24/02,~~ filed on May 24, 2002, now pending. ~~which is a Continuation-In-Part application of serial number 10/058,259, filing date1/29/02, which is a Continuation application of serial number 09/251,183, filing date 2/17/99, now issued as U.S. Patent 6,383,916, which is a Continuation-In-Part application of serial number 09/216,791, filing date 12/21/98, Top Layers Of Metal For High Performance IC's, all of which are herein incorporated by reference in their entity.~~

Please amend the first full paragraph on page 6 as follows:

The present invention adds one or more thick layers of polymer dielectric and one or more layers of thick, wide metal lines on top of the finished device wafer passivation. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 μm. ~~um.~~ The wide metal lines can, for instance, be of electroplated copper or gold. These layers of dielectric and metal lines are of primary benefit for long signal paths and can also be used for power buses or power planes, clock distribution networks, critical signal, re-distribution of I/O pads for flip chip applications. Single, dual and triple damascene techniques, or combinations thereof, are used for forming the metal lines and via fill.

Please amend the first full paragraph on page 10 as follows:

In a key aspect of the invention, the passivation openings can be as small as 0.1 μm. ~~um.~~ In another critical aspect of the invention, various methods are used to form the Post Passivation Technology segment 80, in which metal lines which are formed substantially thicker and wider than those in the IC Interconnection layer. More detail is provided below.

Please amend the third full paragraph on page 10 as follows:

In one important aspect of the current invention, referring now to FIGS. 12a-12h, and specifically FIG. 12a, openings 7 in the polymer layer 5 may be larger than openings 7' in the passivation layer 4. Openings 7' may be formed to as small as 0.1 μm, ~~um,~~ and may range in size from between about 0.1 and 50 μm. ~~um.~~ These small passivation vias 7' are advantageous for the following reasons:

Please amend the first full paragraph on page 14 as follows:

An adhesion layer 200 and an electroplating seed layer 202 are now formed, also as previously described with reference to FIG. 12a, and as shown in FIG. 13. Copper or gold 210 is electroplated up from seed layer 202 to fill openings 7' and 7, as well as above polymer layer 5, as depicted in FIG. 15. Chemical mechanical planarization (CMP) is used to remove the plated metal 210 above polymer 5, stopping on seed layer 202. This forms via

plugs 212 above and connecting to contact points 6, as shown in FIG. 16. Via plugs 212 have a width of between about 1 and 300 μm. ~~um.~~

Please amend the first full paragraph on page 18 as follows:

The following comments relate to the size and the number of the contact points 6, Fig. 1. Because these contact points 6 are located on top of a thin dielectric (layer 3, Fig. 1) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad 6 small. The size of pad 6 is however also directly related with the aspect ratio of via 7. An aspect ratio of about 5 is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad 6 can be in the order of 0.5 μm ~~um.~~ to 3 μm, ~~um.~~ the exact size being dependent on the thickness of layers 4 and 5. ~~The contact points 6 can comprise any appropriate contact material, such as but not limited to tungsten, copper (electroplated or electroless), chromium, aluminum, polysilicon, or the like.~~

Please amend the third full paragraph on page 18 as follows:

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer 4, a layer of approximately 0.2 μm ~~um.~~ PECVD oxide is deposited first followed by a layer of approximately 0.7 μm ~~um.~~ nitride. Passivation layer 4 is very important because it protects the device wafer from

moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metallization structure) is of critical importance since it allows for a cheaper process that possibly has less stringent clean room requirements for the process of creating the interconnecting metallization structure.

Please amend the second full paragraph on page 19 as follows:

Layer 5 is a thick polymer dielectric layer (for example polyimide) that has a thickness in excess of 2 μm ~~um~~ (after curing). The range of polyimide thickness can vary from 2 μm ~~um.~~ to 50 μm, ~~um.~~ dependent on electrical design requirements. The polymer layer 5 is thicker than the intermetal dielectric layers in the interconnecting, fine-line, metallization structure by 2 to 500 times.

Please amend the first full paragraph on page 20 as follows:

The dimensions of opening 7 have previously been discussed. The dimension of the opening together with the dielectric thickness determines the aspect ratio of the opening. The aspect ratio challenges the via etch process and the metal filling capability. This leads to a diameter for opening 7 in the range of approximately 0.5 μm ~~um.~~ to 3.0 μm ~~um.~~ while the height for opening 7 can be in the range of approximately 3 μm ~~um.~~ to 20 μm. ~~um.~~ The aspect ratio of opening 7 is designed such that filling of the via with metal can be accomplished. The via can be filled with CVD metal such as CVD tungsten or CVD copper,

with electro-less nickel, with a damascene metal filling process, with electroplating copper, etc.

Please amend the seventh full paragraph on page 32 as follows:

16) provide a means for more relaxed design rules in designing circuit vias by the application of small passivation (0.1 μm ~~um~~ or more) vias.